Ultra-Low Power Performance Sensor for CMOS Memory Cells

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Abstract

Considering Random Access Memory (RAM), Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) memories, these can be exposed to aging of their components, causing a decrease in their performance, resulting in slower transitions, which in turn will cause slower reads and writes, which can lead to errors during these operations. Therefore, the aging of CMOS memories translates into the occurrence of errors in memories over time, which is undesirable, especially in critical systems. It is therefore necessary to monitor the errors of a memory through sensors.

Another crucial issue for IoT applications is energy management. A wide variety of smart sensors, usually battery operated, require high energy efficiency. This is aimed at searching for ultra-low power microcontrollers and low-power memories. For this, a key variable is the minimum power supply voltage value, V_{DD}, which can ensure secure data retention and access to data (read/write operations). Using a flexible power management unit (PMU), it can be rewarding to perform dynamic voltage and frequency scalling (DVFS) to power memory matrices with minimal V_{DD} during memory access and data retention.

This dissertation aims to present a new sensor (Ultra-Low Power Performance Sensor for Memory Cells), to overcome the problems detected in the Scout Memory Sensor. This sensor is compatible with various types of memory and architectures (SRAM and DRAM) and is a performance sensor that detects the degradation caused by PVTA variations with low power consumption, using DVFS (Dynamic Voltage and Frequency Scaling) techniques, thus allowing its use for lower supply voltages (V_{DD}) in order to save energy. This Ultra-Low Power Performance Sensor for Memory Cells is a novelty compared to the previously proposed sensors, so it has not yet been tested on real circuits.
Keywords: SRAM, DRAM, Performance Sensor, memories

1. Introduction

Internet of Things (IoT) is stimulating the fourth industrial revolution, bringing significant benefits by connecting people, processes, and data [9][10]. The possibility of interconnecting a huge amount of smart hardware/software (hw/sw) systems, with increasing local artificial intelligence, is opening new avenues of research and innovative IoT applications across various markets, from smart cities [11] down to health systems [12], automotive applications [13], aerospace, and so on.

1.1. Hardware Challenges in IoT

One crucial issue for IoT applications is power management [16][17]. A large array of smart sensors, often battery operated, requires high energy efficiency. This quests for ultra-low-power microcontrollers, and low-power memories.

Systems-on-a-Chip (SoCs), and other integrated circuits, today are composed of nanoscale devices that are crammed in a very limited silicon area, presenting reliability issues and new challenges. CMOS circuits' performance is sensitive to parametric variations, such as Process, power-supply Voltage and Temperature (PVT) [1], as well as aging effects (PVT and Aging – PVTA). CMOS circuit's aging degradation is mainly caused by the following effects: Bias Temperature Instability (BTI), Hot-Carrier Injection (HCI), Electromigration (EM) and Time Dependent Dielectric Breakdown (TDDB) [2]. The most relevant aging effect is the BTI, namely the Negative Bias Temperature Instability (NBTI), which affects PMOS MOSFET transistors, resulting in a gradual increase of their absolute threshold voltages over time (—VthP—). As high-k dielectrics started to be employed from the sub-32nm technologies [3], BTI also significantly affects NMOS transistors – Positive Bias Temperature Instability (PBTI), resulting in a rise of their threshold voltages, VthN. These effects degrade digital circuit's performance over time, increasing the variability in CMOS circuits. Perfor-

mance degradation decrease the switching speed, eroding time margins and leading to potential delay faults, and eventually chip failures.

1.2. Motivation

In the past, significant research has been carried out, and a set of cost-effective performance sensors for digital logic, either in a cell-library design style in custom SoCs, or in an FPGA programmable tissue has been proposed (see, e.g., [6][7][18]). However, research on performance sensors for semiconductor memories has been much more limited, so far.

We acknowledge that there is vast previous research dealing with aging sensors for SRAM cells, and especially focused on the BTI effect. These are attempts to increase reliability in SRAM operation. Nevertheless, they do not simultaneously consider PVT and Aging variations. Hence, previous work mainly deals with sensing aging in SRAMs, but a cost-effective generic sensor to deal with performance and, simultaneously, PVTA variations in memories is missing. Moreover, previous work does not address the development of SRAM sensors for ultra-low-power operation, a mandatory request for many IoT applications

1.3. Objectives

The first objective of this work was to study the applicability of work described in [19][20][21], the Scout Memory Sensor, to ultra-low-power circuits, i.e., to study its use under subthreshold power-supply voltage values. The second objective, and the main purpose of this thesis, was to propose changes to the Scout Memory Sensor that could define a novel, ultra-low power, and on-line performance sensor for SRAM and/or DRAM circuits, targeting IoT applications. Furthermore, a final objective of this work was that the time response degradation of a memory circuit with the sensor could be carried out on purpose, to constraint power consumption.

1.4. Context of The Research Work

The research and development of this master's thesis was carried out at the Instituto Superior Técnico (IST) of the University of Lisbon (UL) in collaboration with INESC-ID in Lisbon and University of Algarve – Engineering Institute in Faro.

This work is part of the Master's program in Aerospace Engineering with specialization in the field of avionics and Minor in electronics and telecommunications.

2. CMOS Memories and PVTA Variations

In this chapter we will first make a brief introduction on CMOS memories focusing especially on our attention on the structure of SRAM and DRAM memories, because this work refers to sensors of this type of memories. PVTA effects affecting the performance of CMOS circuits are then summarized. The last section of this chapter describes the use of subthreshold techniques that allow sensors to save more energy, making the process more efficient.

2.1. CMOS Memories

Memory circuits are generally classified according to the type of data storage and the type of data access. *Read-Only Memory* (ROM) circuits allow, as the name implies, only the retrieval of previously stored data and do not permit modifications of the stored information contents during normal operation. ROMs are *non-volatile* memories, i.e., the data storage function is not lost even when the power supply voltage is off.

Read-write (R/W) memory circuits, on the other hand, must permit the modification (writing) of data bits stored in the memory array, as well as their retrieval (reading) on demand. This requires that the data storage function be *volatile*, i.e., the stored data are lost when the power supply voltage is turned off. The read-write memory circuit is commonly called *Random Access Memory* (RAM), mostly due to historical reasons. Compared to sequential-access memories such as magnetic tapes, any cell in the R/W memory array can be accessed with nearly equal access time. Based on the operation type of individual data storage cells, RAMs are classified into two main categories: *Static* RAMs (SRAM) and *Dynamic* RAMs (DRAM).

A typical memory array organization is shown in figure 1. The data storage structure, or core, consists of individual memory cells arranged in an array of horizontal rows and vertical columns. Each *cell* is capable of storing one bit of binary information. Also, each memory cell shares a common connection with the other cells in the same row, and another common connection with the other cells in the same column. In this structure, there are 2^N rows, also called *word lines*, and 2^M columns, also called bit lines. Thus, the total number of memory cells in this array is $2^M \times 2^N$.

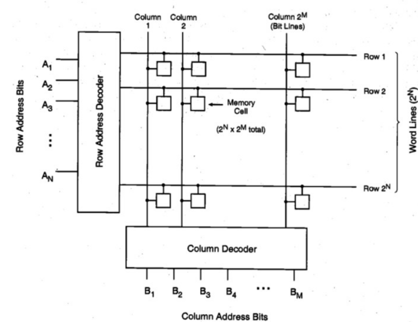

Figure 1: Typical RAM array organization

To access a particular memory cell, i.e., a particular data bit in this array, the corresponding bit line and the corresponding word line must be activated (selected). The row and column selection operations are accomplished by row and column *decoders*, respectively.

2.1.1 SRAM

Read-write (R/W) memory circuits are designed to permit the modification (writing) of data bits to be stored in the memory array, as well as their retrieval (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as a sufficient power supply voltage is provided), without any need for a periodic refresh operation.

The circuit structure of the full CMOS static RAM cell is shown in figure 2, along with the PMOS column pull-up transistors on the complementary bit lines. The most important advantage of this circuit topology is that the static power dissipation is even smaller; essentially, it is limited by the leakage current of the PMOS transistors. A CMOS memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force for the increasing prominence of high- density CMOS SRAMs.

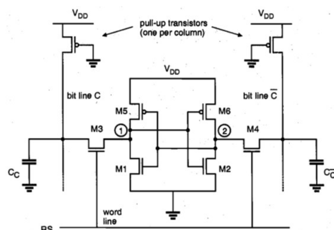

Figure 2: Circuit topology of the CMOS SRAM cell

2.1.2 DRAM

As the trend for high-density RAM arrays forces the memory cell size to shrink, alternative data storage concepts must be considered to accommodate these demands. In a dynamic RAM cell, binary data is stored simply as charge in a capacitor, where the presence or absence of stored charge determines the value of the stored bit. Note that the data stored as charge in a capacitor cannot be retained indefinitely, because the leakage currents eventually remove or modify the stored charge. Thus, all dynamic memory cells require a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur. The use of a capacitor as the primary storage device generally enables the DRAM to be realized on a much smaller silicon area compared to the typical SRAM cell.

2.2. Aging Effects

The challenges of designing integrated circuits (ICs) are focused on accomplishing high reliability and performance, which are partially associated with minimizing aging effects. In MOS technology, the degradation phenomena is classified as destructive and non-destructive, bias-temperature instability (BTI) and hot-carrier injection (HCI) being non-destructive cases and manifesting themselves as charge carrier tunneling from the inversion channel into the gate's dielectric, due to the continuous increasing of vertical and horizontal electric fields. Destructive degradation manifests as electromigration (EM) and time-dependent dielectric breakdown (TDDB), destroying the physical and electrical functionality of interconnections and the MOS's gate insulator [5].

2.2.1 BTI Effect

One major effect of technology scaling to the nanometer scales is reliability challenges [1]–[4]. Among different reliability issues, bias temperature instability (BTI) is the most serious concern [2]–[4]. The BTI gradually increases the absolute value of transistors threshold voltage (V_T) and decreases the mobility (μ) of the charge carriers as well [2], [4].

High electric field on the gate insulator, at the elevated temperature, accelerates BTI phenomenon [5]. When a transistor is in linear or saturation state, electric field on gate insulator that reaches to the millions of volts per meter breaks the Si–H bonds, which had been established at the fabrication time to passivate incomplete bonds between Si and SiO_2. Interface traps that are generated due to this dissociation slow-down the movement of charge carriers. On the other hand, the generated Si ions, due to Si–H bonds break, push the transistor channel away and increase the absolute value of V_T, forming the stress phase of BTI [5], [6]. On the contrary, when the electric field is removed, some of the broken Si–H bonds will be formed again and put the transistor in the recovery phase. In this way, the previous V_T degradation is partially compensated in the recovery phase.

The total effect of BTI is a gradual increase of V_T over time. The amount of V_T degradation is strongly proportional to the duty cycle (the ratio of stress to recovery time), the supply voltage, and the operating temperature [5], [6]. The effect of BTI on p-type and n-type transistors is called NBTI and PBTI, respectively. In the previous fabrication technology sizes, the NBTI has been far more severe than PBTI; however, nowadays by the devel-

opment of high-k materials, the PBTI has become a major concern as well [7], [8].

The main effect of BTI on combinational circuits can be observed as propagation delay increase [9], [10] and the delay variation can be accurately monitored using timing violation sensors [11]–[13]. But, BTI effect on SRAM cells, which occupy up to 90% of processors die area [14], leads to static noise margin (SNM) degradation. The SNM is the minimum noise voltage that can flip the state of the SRAM cell. However, tiny shift in SNM can hardly be monitored using built-in sensors and the sensor precision steps down due to process variation and other environmental parameters change.

2.3. PVT Variations

The continuous shrinking of transistor size leads to great advances in circuit performance besides reducing energy consumption and transistor cost. However, this aggressive scaling also makes the CMOS circuits more susceptible to variability. There exist 3 main sources of variability, namely, Process, Voltage and Temperature (PVT) variations. Process variations are due to the mismatch of the manufacturing process. Voltage variations are mostly due to the parasitic impedance while temperature variations are caused by the power dissipated by the circuit. PVT variations change the transistor switching speed and leakage current.

2.4. Subthreshold Analysis

The Internet of Things (IoT) enables easy access and interaction with a wide variety of devices, some of them self-powered, consisting of microcontrollers, sensors and sensor networks. Therefore, it is important to use power management strategies and reduce power consumption in IoT chips. One of these techniques is the Dynamic Voltage and Frequency Scaling which allows energy to save at subthreshold power supply voltages, but reducing the power supply voltage, implies the reduction of performance and, consequently, delay increase, which turn makes the circuit more vulnerable to operational-induced delay-faults and transient-faults. For this reason, it is important to identify a compromise where power is drastically reduced, but most errors are still avoided or prevented.

3. State of the Art on Performance Sensors

As mentioned in the previous chapter, PVTA variations can result in circuit degradation and consequently failures in RAM memories during their various states of operation. With this in mind, this chapter presents some work done on aging and performance sensors for cells of SRAM and DRAM memories. Unfortunately, there are not many studies on the subject and will be presented only aging sensors caused by the NBTI effect (OCAS), performance sensors for SRAM and an improved version compatible with DRAM memories (Scout Memory Sensor) and finally a sensor for logic circuits (LPS and GPS).

3.1. On-Chip Aging Sensor (OCAS)

On-chip aging sensor (OCAS) is a sensor that permits to detect SRAM aging caused by NBTI effect during system lifetime. The sensor is able to detect any specific aging state of a cell in the SRAM array. The strategy is based on the connection of an OCAS per SRAM column, which periodically performs off-line testing by monitoring write operations into the SRAM cells to detect aging. This approach is application-transparent since it is does not change the SRAM contents after testing. To prevent OCAS from aging by one side and from dissipating static power by the other side, OCAS circuitry is powered-off during idle periods.

In figure 3 is shown the general block diagram of the proposed approach indicating the connection between the OCAS and one SRAM column.

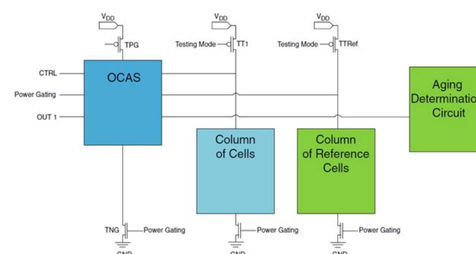

Figure 3: General block diagram of the hardware-based approach connected to one SRAM cell column

3.2. Aging and Performance Sensor for SRAM

In previous works was proposed by Hugo Santos an aging and performance sensor that detects errors when slow transitions in the bit lines occur due to aging effects during write and read operations for SRAM memories.

This sensor is mainly constituted by two blocks as can be seen in figure 4. The first is the transition detector, which generates pulses in the presence of a signal transition, on the memory cell bit lines and the second block is the pulse detector that indicates if the generated pulse (which has a duration proportional to the transition time) exceeds a defined value in the pulse duration, indicating a slow transition and, consequently a critical performance of the memory cell that could lead to a fault. In this case, an error output is generated.

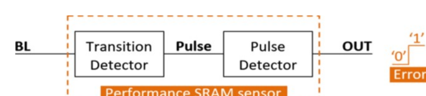

Figure 4: Aging and Performance Sensor block diagram

However, this new sensor still has some disad-

vantages, because this sensor does not apply to DRAM memories, nor does it allow the user to change sensitivity or calibrate it making it more versatile. This sensor also needs to be synchronized with memory, which represents a major limitation for this type of sensor.

3.3. Scout Memory Sensor

A new sensor (Scout Memory Sensor) based on the Hugo Santos sensor, was proposed by Luis Santos, that detects degradation of memory circuits caused by PVTA variations, allowing to avoid the occurrence of errors during read and write operations, signaling appropriately when the performance of memories is at risk. The novelty of this sensor is that it allows its use in SRAM and DRAM memories and also allows the user to calibrate and change the sensitivity of the sensor, making this solution more versatile and solid. Another advantage of this sensor is that it becomes more sensitive if the signal degradation is greater, i.e., its sensitivity is improved when operating conditions are worse. This sensor can be used as a global sensor (monitoring of all memory) or as a local sensor (monitoring of a specific location). Another advantage that this sensor presents is that it can work online, during the normal circuit operation, without the need to go offline.

The Scout Memory Sensor consists of 4 blocks (figure 5) and also features a controller that functions as a Finite State Machine (FSM) with 3 states, *Reset*, *Sample* and *Compare* that allow the control and operation of the entire sensor. The 4 sensor blocks are: the transition detector, the pulse detector, the reference value for comparison and the comparator. The transition detector is connected to the bit line and generates a pulse for each transition that occurs on the bit line. This pulse has a duration proportional to the transition time of the bit line. The pulse detector aims to generate a DC voltage proportional to the pulse duration generated by the transition detector. This pulse detector has a system that allows the user to control sensitivity via 3-bit control. The reference value block creates a reference voltage close to V_{DD} ($V_{DD} - V_T$), for comparison purposes. The last block (comparator) compares the reference voltage with the DC voltage obtained in the pulse detector.

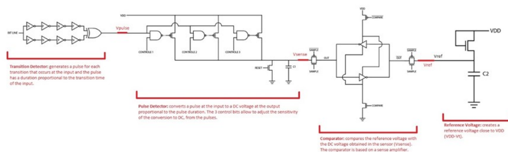

Figure 5: Scout Memory Sensor architecture

3.4. Scout Performance Sensor for Synchronous Circuits

There are aging sensors for synchronous circuits, which can work at subthreshold voltages to considerably reduce power consumption. This type of performance sensor utilizes an adaptive voltage scaling (AVS) strategy to enhance reliability and fault-tolerance and allows circuits to be dynamically optimized during their lifetime while preventing error occurrence.

In this section is made the approach of two types of sensors for synchronous circuits: the local performance sensor (LPS) represented in figure 6, to monitor performance degradations locally, in the actual circuit implementing the mission functionality, in key locations in the circuit where errors are more prone to occur. However, their implementation in a circuit is more complex and performance monitoring can only be done on-line if, and when, the critical paths they monitor are activated, which depends on circuit operation.

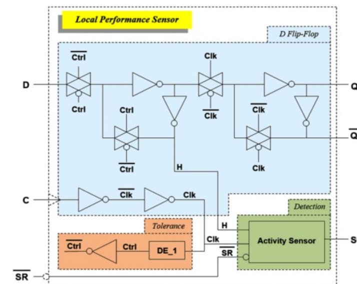

Figure 6: Local Performance Sensor architecture

The other sensor is the global performance sensor (GPS) represented in figure 7, to monitor key critical paths, critical paths' replicas, or key parameters, to detect performance degradation. Their usage in a circuit is very easy and straight forward, because performance monitoring, normally, is independent from circuit operation, which is why they are easily adopted by industry. However, they do not monitor circuit at the actual locations where error occur, and, because of that, their estimated Process, Voltage, Temperature and Aging (PVTA) variations may differ from the ones that in the real circuit can produce an error.

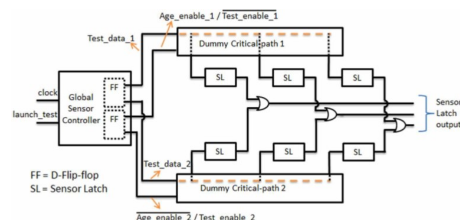

Figure 7: Global Performance Sensor architecture

In order to optimize energy efficiency, we can use GPS and LPS together, that allows an ultra-

low power strategy for reliable IoE nanoscale digital circuits.

4. Study of Scout Memory Sensor for Subthreshold Voltages

In this chapter is made the study of the Scout Memory Sensor (presented in chapter 3) for supply voltages below the nominal voltage as is the case of the subthreshold regime. This chapter pretends to know if for lower voltages, the Scout Memory Sensor is still a robust solution, presenting reliable behavior and what the minimum supply voltage for which the sensor is reliable.

In this chapter is analyzed the operation of each block of the Scout Memory Sensor, namely the transition detector, the pulse detector and also the complete circuit of the sensor. Some simulations were made using Cadence software and UMC130 technology.

4.1. Simulation Results

To study the sensor behavior for low supply voltage, a parametric simulation of the 4 sensor blocks was performed for a bit line of "Low" to "High" with a rise time of 700 ps. Capacitors with capacities C1=17 fF, C2=100 fF, transistors with size WNmin=160 nm, WPmin=600 nm and the three control bits activated were used.

The results are displayed in a graphic and in a table for $Vdd \in [0,2V;1,2V]$ values

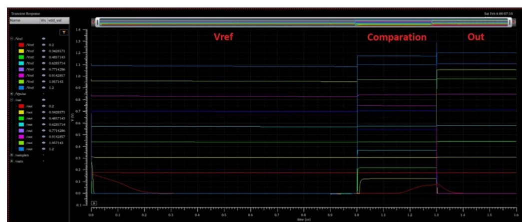

Figure 8: Parametric analysis of the complete circuit for $Vdd \in [0,2V;1,2V]$

4.2. Scout Memory Sensor Analysis

Through the simulations carried out we can conclude that the transition detector and pulse detector blocks still work under subthreshold, and the minimum supply voltage for which the sensor still works is 0.11 V. In the subthreshold regime, the transition detector can still generate a pulse, albeit with a high delay. But simulations also show that the comparator block presents problems for subthreshold voltages due to the complexity of its architecture and the stack of electronic components. The Scout Memory Sensor is no longer consistent and coherent in the subthreshold regime, as it does not guarantee error signaling when supply voltages are very low for too slow bit line transitions. In addition, for very low supply voltages the difference between the Vsense and Vref signals becomes too small for the comparator block to function properly.

For these reasons, the Scout Memory Sensor is an incomplete sensor and fails under certain conditions. Therefore, it is necessary to find an alternative to this sensor that works at lower supply voltages. This dissertation aims to present new solutions to the problems verified in the Scout Memory Sensor and we can also take advantage of the transition detector block, because this block works correctly under subthreshold.

5. Ultra-Low Power Performance Sensor for Memories

In this chapter is presented a new sensor to overcome the problems detected in the Scout Memory Sensor (chapter 4). This sensor is compatible with various types of memory and architectures (SRAM and DRAM) and is a performance sensor that detects the degradation caused by PVTA variations with low power consumption, using DVFS (Dynamic Voltage and Frequency Scaling) techniques, thus allowing its use for smaller supply voltages (V_{DD}) in order to save energy. This Ultra-lLow Power Performance Sensor is a novelty compared to the previously proposed sensors, so it has not yet been tested on real circuits.

5.1. Sensor Architecture

In this subsection is presented the complete circuit of the Ultra-Low Power Performance Sensor (figure 9).

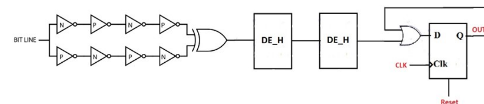

Figure 9: Complete circuit for Ultra-Low Power Performance Sensor

As we can see the sensor consists of the transition detector block, two delay elements and a flip-flop block. This sensor signals signal degradation during Read/Write operations in a memory cell due to PVTA variations. For this the sensor uses a map of delays of the signals that are added successively. Due to the occurrence of PVTA variations, these delays increase in size and when the total number of delays reaches the second rising edge of the flip-flop clock, the sensor signals an error, indicating that the normal operation of the memory is on the imminence of failure.

The sensor detects a transition from the bit line and generates a pulse proportional to the transition time. Due to the presence of delay elements, a delay is added to the pulse, to simulate the delay that occurred during the use of the data written/read by another logic combinatorial of the circuit. Then a flip-flop is used to detect the pulse when it reaches

Vdd	Pulse Delay	Pulse Width	VSense	Vref	Out	VSense in % of Vdd	Vref in % Vdd
$1,2$ V	$388,99$ ps	$248,55$ ps	$1,17$ V	$1,09$ V	$1,2$ V	$97,94$ %	$91,13$ %
$1,06$ V	$427,81$ ps	$238,37$ ps	971 mV	965 mV	$1,06$ V	$91,6$ %	$91,04$ %
$0,91$ V	$478,04$ ps	$239,71$ ps	749 mV	828 mV	$8,66\ \mu V$	$82,31$ %	$90,99$ %
$0,77$ V	$546,32$ ps	$267,45$ ps	545 mV	699 mV	$3,82\ \mu V$	$79,78$ %	$90,78$ %
$0,63$ V	$708,81$ ps	$357,28$ ps	368 mV	569 mV	$4,14\ \mu V$	$58,41$ %	$90,32$ %
$0,49$ V	$1,11$ ns	$725,07$ ps	220 mV	438 mV	$6,52\ \mu V$	$44,9$ %	$89,39$ %
$0,34$ V	$4,46$ ns	$4,55$ ns	127 mV	302 mV	$4,14\ \mu V$	$37,35$ %	$88,82$ %
$0,2$ V	$77,68$ ns	$98,09$ ns	75 mV	176 mV	$6,52\ \mu V$	$37,54$ %	88 %

Table 1: Parametric analysis data of the complete circuit for $Vdd \in [0,2V;1,2V]$

the second rising edge of the clock.

As already mentioned above, this sensor uses a DVFS technique to be used for low supply voltages. The purpose of this technique is to correspond for each V_{DD} value, a different frequency from the clock, so that the sensor works at maximum performance (i.e., on the imminence of an error), ensuring that the safety margin remains for all V_{DD} levels.

5.2. Usability Analysis and Conclusion

The sensor presented in this chapter can be used in SRAM and DRAM memories and for any type of architecture of the memory cell, because the sensor works as long as transitions occur in the bit line. This sensor works for low supply voltages up to 0.33V, from which the memory cell stops working properly and the use of the sensor becomes inappropriate.

This sensor is quite versatile because it allows the designer to use different types of transition detector blocks and delay element blocks. If greater safety margin is required, the designer can increase the number of inverters used in the transition detector to obtain wider pulses. On the other hand, if data from memory is captured by a more complex combinatorial logic that requires greater delay, the designer can use more delay elements.

5.2.1 Local Sensor vs Global Sensor

When it is necessary to download the V_{DD}, I use the DVFS controller, to slowly lower the frequency, but the circuit has local sensors that are detecting whenever there is a violation of the safety margin, which means that the circuit has aged, so the V_{DD} that is working, no longer works for the respective frequency of the table, so that means that the frequencies have to be adapted whenever the local sensor detects an error. The values of the DVFS controller table are already optimized pairs, i.e., for a given V_{DD} and clock frequency, if anything varies the sensor indicates an error. If however local sensors detect an error, then the controller updates the table values and passes to new V_{DD} pairs and clock frequency.

You can also add a global sensor that is constantly or periodically monitoring a dummy memory cell to see if there have been errors. Whenever an error occurs in the dummy memory cell, the DVFS controller table is updated. This may be important in the case where the main circuit is not in use and so the table is not being updated, so it makes sense to use a global sensor to monitor whenever needed and along a local sensor to monitor whenever the main circuit is working.

5.2.2 Advantages and Disadvantages

The Ultra-Low Power Performance Sensor has the advantage of being a more robust sensor than the main circuit, to work better than the main circuit. Another advantage is that the simpler the sensor the longer the delay and the more cautious it is, so it means that if operating conditions are worse (more aging, lower V_{DD}, higher temperature), the sensor becomes even more cautious, preventing errors more easily.

The sensor presented in this chapter is a performance sensor that detects errors regardless of their origin (Process, Supply Voltage, Temperature and Aging), because the error is reflected only in the speed of transition of the bit line

An disadvantage of this sensor is that if I use a clock with a large period, it may be necessary to use many delay elements to be able to increase the delay and produce the pulse near the second rising edge of the clock, considerably increasing the sensor area. On the other hand the existence of a flip-flop also increases the area, because the flip-flop is a cell that has 18 transistors, which means that it is a relatively large cell, implying a larger sensor, so it should not be connected to all bit lines.

6. Implementation Layouts

In this section, the layouts for the memories and performance sensors are presented. First, we present the layout implementation of a sample memory, in this case an SRAM memory. Then, the layout for the Ultra-Low Power Performance Sen-

sor is also presented, highlighting each constituent block of the sensor. Finally, the layout for the complete circuit of a 1-bit SRAM memory with the sensor.

The analysis of the layouts allows us to understand the dimensions and surface area of the circuits and their blocks. To perform these layouts, Cadence software and UMC130nm technology were used.

6.1. 1-Bit SRAM

Figure 10 shows the complete 1-bit SRAM layout, consisting of the four blocks already mentioned. In the layout the top track is the V_{DD} and the bottom track is the ground (gnd). The light blue connections are in metal 1, in yellow they are in metal 2 and white in metal 5. The bit line (BL) is at the top and the complementary bit line (BLn) is located below. This circuit has five inputs (WL, Sense, Pre_Charge, Write_Data and Write_Enable).

The complete 1-bit SRAM characteristics are:

– Width: 32,7 μm (3270 lambda);
– Height: 11,8 μm (1180 lambda);
– Surface area: 385,86 μm^2.

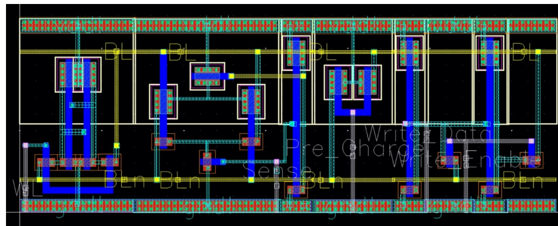

Figure 10: Complete 1-bit SRAM layout.

6.2. Ultra-Low Power Performance Sensor

Figure 11 shows the complete layout of the Ultra-Low Power Performance Sensor with the three building blocks (transition detector, delay element and flip-flop). In the layout the top track is the V_{DD} and the bottom track is the ground (gnd). The light blue connections are in metal 1, in yellow they are in metal 2, the green is in metal 3, purple in metal 4 and white are in metal 5. This circuit has as inputs: bit line (BL), Clock, Reset; and as output: the OUT signal.

The characteristics of the complete sensor are:

– Width: 72 μm (7200 lambda);
– Height: 11,8 μm (1180 lambda);
– Surface area: 849,6 μm^2.

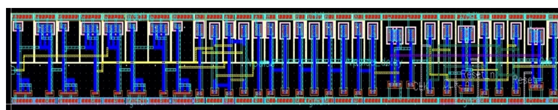

Figure 11: Complete sensor layout.

6.3. 1-Bit SRAM With Ultra-Low Power Performance Sensor

To analyze the total size of the circuit, figure 12 shows the layout of the 1-bit SRAM memory (left side) along with the Ultra-Low Power Performance Sensor (right side). In the layout the top track is the V_{DD} and the bottom track is the ground (gnd). The light blue connections are in metal 1, in yellow they are in metal 2, the green is in metal 3, purple in metal 4 and white are in metal 5. This circuit has as inputs the signals: Word Line, Sense, Pre_Charge, Write_Data, Write_Enable, Clock, Reset; and as output: the OUT signal.

The characteristics of the 1-bit SRAM with Ultra-Low Power Performance Sensor are:

– Width: 104,6 μm (10455 lambda);
– Height: 11,8 μm (1180 lambda);
– Surface area: 1234,3 μm^2.

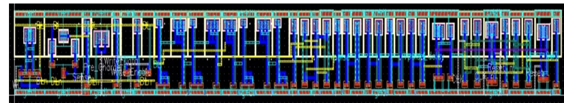

Figure 12: 1-bit SRAM plus Ultra-Low Power Performance Sensor layout.

7. Conclusions

This master's thesis is another step forward in the search for a performance sensor for memories (SRAM and DRAM), to detect errors during read and write operations. The purpose is to make a sensor that can be used in the subthreshold regime.

7.1. Conclusions for Scout Memory Sensor at Subthreshold Regime

The first objective of this dissertation involved the analysis of the behavior of the Scout Memory Sensor (developed by Luis Santos in [19]) to work at lower supply voltages and close to threshold voltage (V_T) (subthreshold regime). For this, several parametric simulations of the different constituent blocks of the Scout Memory Sensor were performed. Through the simulations carried out, we can conclude that the first two blocks of the sensor (transition detector and pulse detector) work well in the subthreshold regime up to supply voltages of 0.11V. However, regarding the comparator block, the simulations showed that this block has failures when working in the subthreshold regime, because this block becomes incoherent, signaling errors at higher supply voltages and, for lower supply voltages, these errors are no longer signaled.

7.2. Conclusions for the new Ultra-Low Power Performance Sensor for memories, at Subthreshold Regime

The Ultra-Low Power Performance Sensor has a different operation and simpler architecture when compared with the Scout Memory Sensor. This fact makes its use more appropriate for working at a subthreshold voltage regime.

Through the simulations presented in this dissertation, we can conclude that this sensor works

well for supply voltages in the subthreshold regime (namely up to 0.33 V). However, it is advised to work up to supply voltages close to 0.4 V, because below this value the sensor is no longer so cautious (decreasing the percentage of safety margin). The sensor can signal errors due to PVTA variations from the cell or from the peripheral circuits of the memory. On the other hand, this sensor can be used both in SRAM and DRAM memories, and most important for any type of memory cell architecture, because the sensor works as long as transitions occur in the bit line. Moreover, this version can be used as a local sensor, placed inside the memory, placed in all bit lines, or monitoring a small sample of cells to reduce area overhead. Also, it can be used to design a complete global sensor approach.

7.3. Future Work

As in all the works there is always something that remains to be developed and in this section it is intended to mention works that can be carried out in the future. Future works are:

- One of these future works is to perform tests and simulations for the Ultra-Low Power Performance Sensor for writings or readings in a different SRAM memory cell than type 6T (as is the case with 8T and 10T memory cells) and verify that the sensor continues to have the same reliability and robustness.
- A new implementation of the sensor transition detector when working with SRAM memories can be done as future work, and the existing transition detector can be simplified. In resume, we can replace the fastest path of the unbalanced inverters (path 1) with a direct line connected to the XOR gate, because the SRAM is initialized to V_{DD}.
- Another future work is the development of a DVFS controller that allows the sensor to operate at low voltages, namely under subthreshold regime, to establish the V_{DD} / f_{CLK} optimum pairs.
- On the other hand, it is necessary to implement the sensor as a global sensor, with its circuitry, including a dummy memory, sensors, and a controller.
- An important future work is to change the delay element block in order to include a sensibility control to the sensor, i.e., to allow the propagation delay of the delay element to be changed during online operation.
- Finally, a work to be carried out in the future is the implementation of the sensor in a chip, with the aim of being possible to validate in silicon all sensor functionalities described.

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